Amendments to the Claims:

1.(currently amended) A clock system comprising:

a receiver circuit for receiving a binary coded time signal, comprising:

a microprocessor clock unit connected to said receiver circuit and which includes programming for a first running time update associated with a first frequency and a separate second running time update associated with a second frequency to enable energization of said receiver circuit for a minimum time period necessary to receive said binary coded time signal in said first frequency for said first running time update and upon failure of receipt of said first frequency to enable <u>serial</u> energization of said receiver circuit for a minimum time period necessary to receive said binary coded time signal in said second frequency for said second running time update, said microprocessor clock unit programmed to energize said receiver circuit for a minimum time period associated with each of said first and said second frequencies, necessary to receive said binary coded time signal, and to shut said receiver circuit off after said minimum time period; and

a clock display connected to said microprocessor clock unit for displaying time.

2.(original) The clock system as recited in claim 1 wherein said minimum time period necessary to receive said binary coded time signal is sufficient to insure receipt of a full one minute time signal within said minimum time period.

3.(original) The clock system as recited in claim 1 wherein said minimum time period necessary to receive said binary coded time signal is sufficient to insure receipt of a small portion of a full one minute time signal necessary to provide a time update having a magnitude of no more than five seconds.

4.(canceled) The clock system as recited in claim 1 wherein said microprocessor clock unit includes programming for a separate first time storage and a separate second time storage and retrieval to enable a user to energize said receiver circuit for a minimum time period necessary to receive said binary coded time signal in said first time storage and without disrupting said second time storage.

5.(canceled) The clock system as recited in claim 4 wherein said separate first time storage and said separate second time storage are each associated with a separate binary coded time signal.

6.(previously presented) The clock system as recited in claim 4 wherein an elapse of time of said microprocessor clock unit is not disrupted in absence of receipt of said binary coded time signal.

7.(previously presented) The clock system as recited in claim 1 wherein said programming is such that and upon failure of receipt of said second frequency said receiver circuit is energized for a minimum time period necessary to receive said binary coded time signal in said first frequency for said first running time update.